

ACKNOWLEDGEMENT RECEIPT

Electronic Version

Stylesheet Version v01

Title of Invention

METHOD FOR SEPARATELY OPTIMIZING THIN GATE
DIELECTRIC OF PMOS AND NMOS TRANSISTORS WITHIN THE
SAME SEMICONDUCTOR CHIP AND DEVICE MANUFACTURED
THEREBY

Submission Type : Utility Patent Filing

Application Number:

10/605110



EFS ID:

47412

Server Response:

Confirmation Code	Message
ISVR1	Submission was successfully submitted - Even if Informational or Warning Messages appear below, please do not resubmit this application
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First Named Applicant: Anthony Chou

Attorney Docket Number: FIS920030228US1

Timestamp: 2003-09-09 16:12:44 EDT

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File Listing:

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